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Survey on Topologies, and Control Techniques for the Most commom Multilevel Inverters

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Abstract— Multilevel inverters have been attracting in favor of industry as well as academia recently for highand medium power applications. In addition, switched waveforms can be synthesized by multilevel inverters in order to achieve lower levels of harmonic distortion than an equivalently rated two-level converter. Decreasing the harmonic distortion in the output waveform can be achieved by using multilevel inverter topology without decreasing the inverter power output. Moreover, multilevel inverter have the ability to generate high quality output waveforms with a low switching frequency. This paper presents the most important topologies like Modular Multilevel Converter (MMC), Neutral Point Clamped Multilevel Inverter (NPCMLI), Clamped/Flying Capacitor Multilevel Inverter (CCMLI), and Cascaded H-Bridges Multilevel Inverter (CHMLI). This paper also presents the comparison between four types of multilevel inverter in Total Harmonics Distortion (THD) and Individual rating comparison. Also, this paper shows FFT the simulation results for THD. Authors strongly believe that this survey article will be very much useful to the researchers for finding out the relevant references in the field of topologies and modulation strategies of multilevel inverter.

Index Terms SVPWM Modular Multilevel Converter (MMC), Neutral Point Clamped Multilevel Inverter (NPCMLI), Clamped/Flying Capacitor Multilevel Inverter (CCMLI), and Cascaded H-Bridges Multilevel Inverter (CHMLI).

1 MULTILEVEL CONCEPT

The general principle of three main types of multilevel inverters will be presented and their behavior introduced in this chapter. Figure 1 shows how multilevel inverters work. Figure 1-a shows the leg of a 2-level converter in which an ideal switch is used instead of semiconductor switches. The output voltage can have only two values: 0 or E. Considering Figure 1-b, the output voltage of a 3-level inverter leg can be three values: 0, E or 2E. Figure 1-c represents a generalized n-level inverter leg. Even in this circuit, n different voltage levels to the output can be provided and an ideal switch can be used instead of the semiconductor switches. Some simplifications will be introduced to get deep understanding of multilevel inverters' circuits. A three-phase multilevel inverter composed of n-level legs will be considered for the analysis. Obviously, the number of phase voltage output levels is n. The number k of the line-to-line voltage levels can be given by (1).

$$k=2n-1 \qquad (1)$$

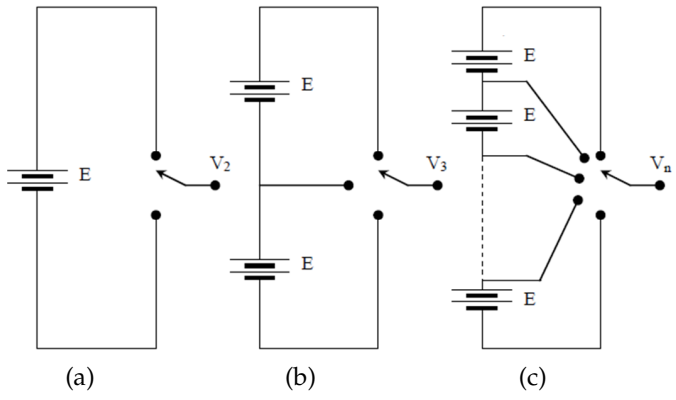

Fig. 1. Inverter phases. (a) 2-level inverter, (b) 3-level inverter, (c) n-level inverter

Figure 2 shows a 2-level inverter; such inverters are mostly used today to generate an AC voltage from a DC voltage. Two different output voltages for the load, V_dc/2 or -V_dc/2, can be created. The concept of multilevel inverters depends on several voltage levels that are added to each other to create a smoother stepped waveform which is closer to a pure sinusoidal waveform; Figure 3 shows that with an increase in the number of output voltage levels, lower dv/dt and lower harmonic distortions can be achieved. With more voltage levels in the inverter, the waveform becomes smoother, but the design and its controller will be more complicated, with many levels with more components.

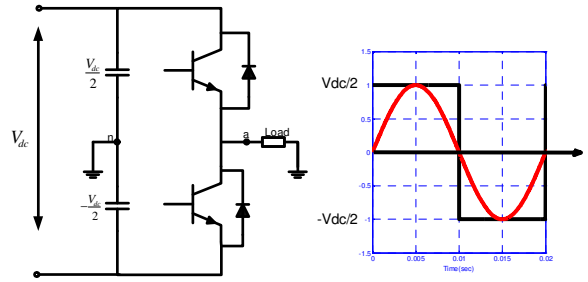

Fig. 2. One phase leg of a 2-level inverter and a 2-level waveform without PWM

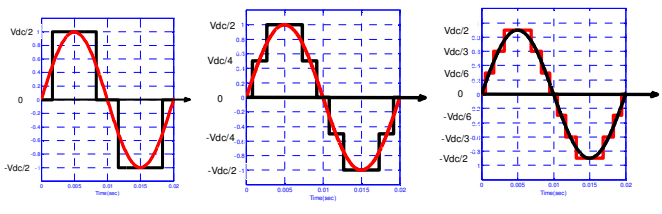

Fig. 3. A 3-level waveform, a 5-level waveform and a 7-level multilevel

To offer deep understanding of multilevel inverters, the 3-level inverter, shown in Figure 4, can be described. Every phase leg can generate the three voltages, $\frac{V_{dc}}{2}$, 0, $-\frac{V_{dc}}{2}$, as can be seen in the first part of Figure 1.4. For a 3-level inverter design, there are twice as many valves in each phase leg. There are diodes in between the upper and lower two valves, called clamping diodes, connected to a neutral midpoint in between two capacitors, as can be seen in Figure 4. The capacitors build up the DC bus; each capacitor can hold the voltage $\frac{V_{dc}}{2}$. Together with another phase leg, connected to the neutral point n, an output line-to-line voltage will have more levels.

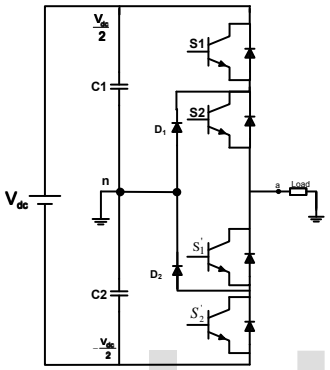

Fig. 4. One phase leg of a 3-level inverter

Zero voltage can be generated by switching on the two switches closest to the midpoint, and the clamping diodes hold the voltage to zero with the neutral point. The inverter can generate even more voltage levels by adding more switch pairs, clamping diodes and capacitors; according to Figure 3, the result is a multilevel inverter with clamping diode topology. The switching losses can be reduced by reducing the switching frequency, and the dv/dt also will be reduced, as can be seen in Figure 3 as the number of levels increase. More stepped output voltage waveforms can be generated by three different kinds of topologies of multilevel inverters and that are suitable for different applications. Multilevel inverter circuit topologies with different configurations have been developed to provide different designs, some of which will be studied in this chapter. The multilevel inverter topologies Neutral-Point Clamped Multilevel Inverter (NPCMLI), Capacitor Clamped Multilevel Inverter (CCMLI) and Cascaded Multilevel Inverter (CMLI) and Modular Multilevel Converter (MMC) will be investigated in this paper

2 Neutral Point Clamped Multilevel Inverter, NPCMLI

As can be seen in Figure 5, this topology is based on the same principle as mentioned before, the 3-level inverter in Figure 4. Using voltage clamping diodes is essential in the NPCMLI topology. An even number of bulk capacitors in a series with a neutral point in the middle of the line is used to divide a common DC bus and depends on the number of output voltage levels in the inverter, as can be seen in the left part of Figure 5. From the DC bus, with neutral point and capacitors, n-1 number of switches pairs are connected to clamping diodes, where n is the number of voltage levels in the inverter (voltage levels that can be generated). Figure 5 shows one phase leg of a 5-level NPC inverter. Three phase circuits can be generated by adding two identical circuits of phase legs sharing the DC bus. Because all diodes have to be of the same voltage rating and are able to block the required number of voltage levels, they are connected in a series. To illustrate, all diodes are rated for $\frac{V_{dc}}{n-1}$, and in Figure 5 all rated diodes are $\frac{V_{dc}}{4}$. The D1´ diodes have to block $\frac{3V_{dc}}{4}$, so there are three diodes in a series. With the same configuration for other steps, 5-levels of voltage can be generated between point a and the neutral point n, and the voltage steps are $\frac{V_{dc}}{2}$, $\frac{V_{dc}}{4}$, 0, $-\frac{V_{dc}}{4}$, and $-\frac{V_{dc}}{2}$, depending on the status of switches that are switched on or off. The waveform of the output voltage for one phase leg of the inverter can also be seen in Figure 5, in which the steps are clearly visible. The steps will be smaller, and the waveform will be closer to a sinusoidal signal. However, the number of needed components and the complexity of the inverter will be increased with a higher number of voltage levels.

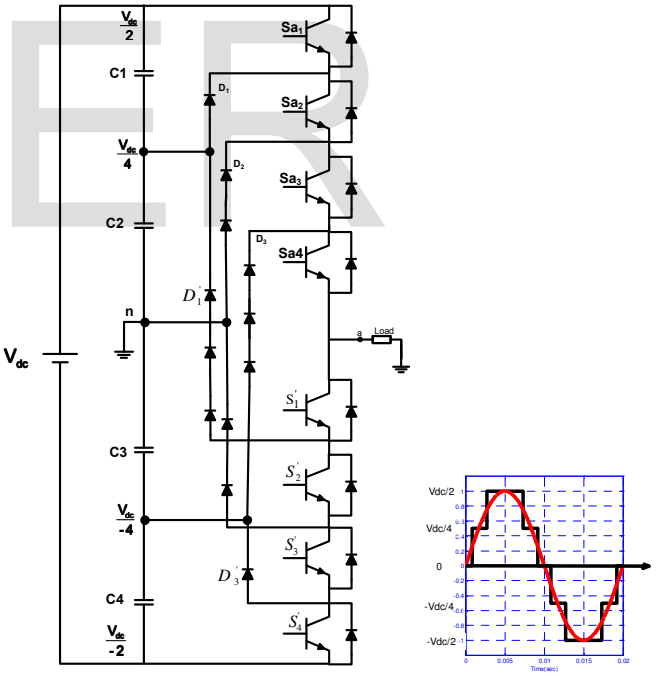

Fig. 5 One phase leg for a 5-level NPC Inverter with its output voltage steps

A setup of switching state combinations has to be used to generate the different voltage levels in the output waveform. Table 1 shows the different states for the 5-level NPC inverter. Note that every switch will turn on (and off) once per cycle, which means a stepped sinusoidal waveform with a fundamental switching frequency can be generated by the inverter. Table 1 shows that for the voltage $\frac{V_{dc}}{2}$ all the upper switches have to be turned on, connecting point a to the $\frac{V_{dc}}{2}$

potential. For the output voltage $\frac{V_{dc}}{4}$, the surrounding clamping diodes D1 and D1' help switches S2, S3, S4 and S1' when they are turned on to hold the voltage. Clamping diodes D2 and D2' or D3 and D3' hold the voltage form voltage levels $-\frac{V_{dc}}{4}$ and $-\frac{V_{dc}}{2}$, respectively. The current goes through the four top or bottom switches when the voltages are $\pm\frac{V_{dc}}{2}$.

TABLE 1
SWITCHING STATES OF ONE 5-LEVEL PHASE LEG. A "1" MEANS TURNED ON AND "0" MEANS TURNED OFF.

Output voltage	S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'
$\frac{V_{dc}}{2}$	1	1	1	1	0	0	0	0
$\frac{V_{dc}}{4}$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-\frac{V_{dc}}{4}$	0	0	0	1	1	1	1	0
$-\frac{V_{dc}}{2}$	0	0	0	0	1	1	1	1

When the current is positive, while voltage is positive, it will go through the Dx diodes, and when the current is negative, it will go through the Dx' diodes and also through the switches in between the clamping diodes and the load. For example, when the voltage is $\frac{V_{dc}}{4}$ and the current is positive, it will go through diode D1 and switches S2, S3 and S4. To keep the DC bus constant, the DC source is used to charge the DC bus. Therefore, currents are flowing through the DC bus. As can be seen from Table 1, some switches are on more frequently than others in order to generate a sinusoidal output wave that requires the use of all voltage levels, and mainly S4 and S1' are used for that purpose. Since the capacitors are charged and discharged unequally and the current is drawn from nodes between capacitors, this leads to unbalanced capacitor voltages when the inverter is transferring active power. The capacitor voltages will deviate from each other, while the total DC bus voltage will be the same.

Since the inner switches are used in several of the switching states, the inner switches are on more frequently than the switching status for the outer switches. Therefore, a different amount of RMS current will be flow through the switches depending on their status, and because the inner switches have a higher current rating, switches with a higher rating are needed for this purpose. Different levels of reverse voltage, depending on where they are connected, have to be blocked by clamping diodes, so the position of the clamping diodes is very important to their ratings. Because of the extra blocking diodes, the NPC topology is unpractical with higher amounts of voltage levels, and the number of diodes grows quadratically with the level n following the equation $(n - 1) * (n - 2)$ [1]. Based on the above explanation, all of the components (n - 1) DC capacitors, 2(n - 1) main diodes and 2(n - 1) switches are required for the NPCMLI topology. For a three-phase inverter of the NPC type, all components are multiplied by three except the DC bus, which can be shared, and only the (n - 1) DC-capacitors mentioned are needed. The general n-level a-phase diode-clamped structure is shown in Figure 6. Therein, only the upper half of the inverter is considered because the lower half contains complementary switches and may be analyzed in a similar way [3].

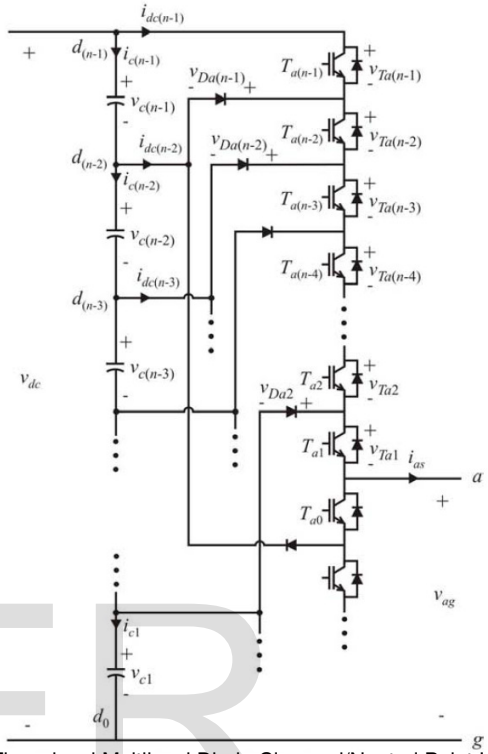

Fig. 6. The n-level Multilevel Diode Clamped/Neutral Point Inverter, NPCMLI [3]

3 CLAMPED/FLYING CAPACITOR MULTILEVEL INVERTER, CCMLI

Figure 7 shows a Capacitor Clamped (CC), or Flying Capacitor, multilevel inverter topology, which has a similar topology to the NPCMLI topology. It uses capacitors to hold the voltages to the desired values instead of using clamping diodes. Like NPCMLI, CCMLI has n-1 capacitors on a shared DC bus, where n is the output voltage level number of the inverter and 2(n-1) switches pairs are used. However, for the CCMLI, instead of clamping diodes, one or more capacitors are used to create the output voltages. They are connected to the midpoints of two switch pairs in the same position on each side of the midpoint between the valves [1]; see capacitors C1, C2 and C3 in Figure 1.19. As can be seen from Figure 7, the numbers of main switches and DC bus capacitors are used for the CCMLI as well as the NPCMLI. The number of switching combinations will be increased because capacitors do not block reverse voltages [1]. The same voltage levels can be generated by the same several switching. One or more of the clamping capacitors voltages are added together in order to generate output voltage by the DC bus voltage $\pm\frac{V_{dc}}{2}$. Generally, every capacitor is rated for the voltage $\frac{V_{dc}}{n-1}$. Therefore, every capacitor is rated for the voltage $\frac{V_{dc}}{4}$ for the 5-level case. To

illustrate, $\frac{V_{dc}}{4}$ is generated by the DC bus positive top value ($\frac{V_{dc}}{2}$) and the reverse voltage of clamping capacitor C1. By helping other clamping capacitors, the other voltage states work in similar ways. The level of CCMLI switching status is shown in Table 2.

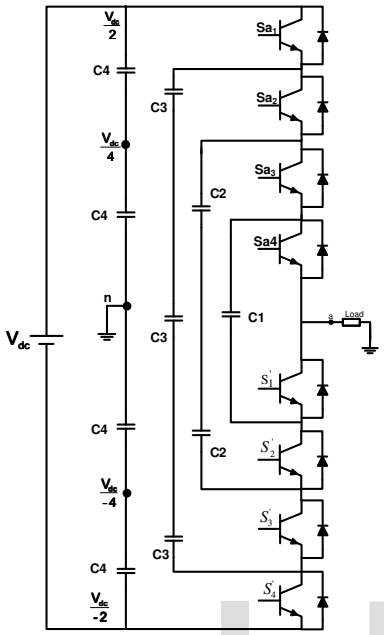

Fig. 7. A Capacitor Clamped Multilevel Inverter with five voltage levels

To change one state to another, only one switch needs to be turned on and one turned off. Table 2 also shows switching states for the 5-level case, but these states are not the only states that put out these voltages. There are several switching states for all of the voltage levels, except the $\pm\frac{V_{dc}}{2}$ states. The capacitors can charge or discharge each other depending upon which switching state is chosen, making it possible to balance the charge in the capacitors with control methods [2]. The energy can be transferred from more charged to less charged capacitors when the same current flows through all the active capacitors in a state, and this leads to a balance of the capacitor voltages among the capacitors that are conducting.

TABLE 2
SWITCHING STATES OF A 5-LEVEL CCMLI PHASE LEG. A "1" MEANS TURNED ON AND "0" MEANS TURNED OFF.

Output voltage	S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'
$\frac{V_{dc}}{2}$	1	1	1	1	0	0	0	0
$\frac{V_{dc}}{4}$	1	1	1	0	1	0	0	0
0	1	1	0	0	1	1	0	0
$-\frac{V_{dc}}{4}$	1	0	0	0	1	1	1	0
$-\frac{V_{dc}}{2}$	0	0	0	0	1	1	1	1

Some states take a long time, and the active capacitors get discharged or charged more than the other capacitors. Therefore, the capacitors' voltages are unbalanced while transferring active power. The CCMLI topology is very similar to that of NPCMLI. The components needed for CCMLI are (n - 1) capacitors on a shared DC bus and 2(n - 1) switch pairs, but CCMLI topology uses clamping capacitors instead of diodes. These capacitors do what the diodes did. Therefore, the number of required components grows quadratically with the voltage level n, following the equation $\frac{(n-1)*(n-2)}{2}$ [1], not counting the main capacitors on the DC bus. Because of the high voltage ratings, the topology requires as many components of the same sort and rating in a series as the clamping diodes have. As in the NPCMLI, the DC bus can be shared when CCMI is used as a three-phase system and all the remaining components are only multiplied by three.The general n-level a-phase Capacitor Clamped structure is shown in Figure 8. Therein, only the upper half of the inverter is considered because the lower half contains complementary switches and may be analyzed in a similar way [3].

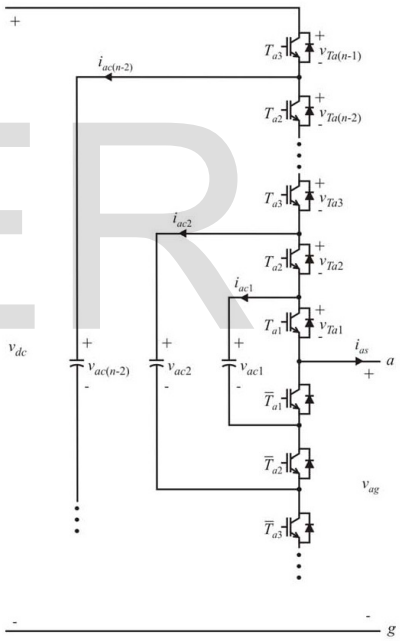

Fig. 8. The n-level Multilevel Capacitor Clamped/Flying Capacitor Inverter, CCMLI [3]

4 CASCADED H-BRIDGES MULTILEVEL INVERTER CHMLI

A single-phase structure of an n-level cascaded inverter is illustrated in Figure 9 [3]. Each separate DC source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Three different voltage outputs, +Vdc, 0 and –Vdc, can be generated by each inverter level by using the different combinations of four switches, S1, S2, S3 and S4, to connect dc source to ac output. By switching S1 and S4 on, the voltage will be +Vdc, whereas –Vdc can be obtained by turning on switches S2 and S3. The output voltage 0 can be obtained by

turning on S1 and S2 or S3 and S4. The voltage waveform generated is the sum of the inverter outputs of each of the different full-bridge inverter levels when they are connected in a series. The number of output phase voltage levels n in a cascade inverter is defined by n = 2s+1, where s is the number of separate dc sources. An example phase voltage waveform for an 11-level cascaded H-bridge inverter with 5 SDCSs and 5 full bridges van = va1 + va2 + va3 + va4 + va5. Comparing the NPCMLI, CCMLI and CHMI, fewer components are required in CHMI, and the same number of components can be used to generate every voltage level. However, the number of required sources can be determined by $s = \frac{n-1}{2}$. Therefore, when the output voltage level increases, the number of sources increases. CHMI requires the same number of sources s and the number of full-bridge modules. Every full-bridge module has four switches in turn, giving the CHMI $4 * \frac{n-1}{2} = 2(n-1) = 4s$ switches. The number of needed components needs to be multiplied by three for all components for a three-phase CHMI topology inverter and when there is no common DC bus to share.

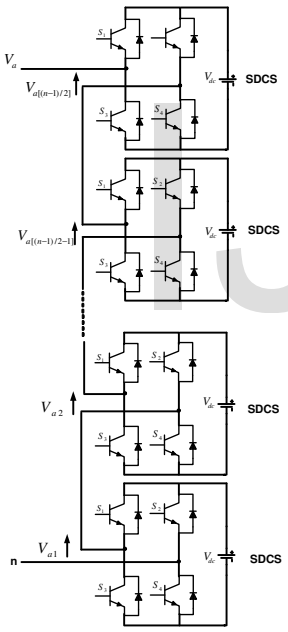

Fig. 9. Single-phase structure of a cascaded H-bridges multilevel inverter

5 Modular Multilevel Converter, MMC

The MMC had been invented by A. Lesnicar and R. Marquardt as a development from the Cascaded H-Bridge Converter [20]. Because of its modular structure, the MMC has received great attention because its modularity and expandability are used for high-power applications and it has many advantages as a multilevel inverter. Currently, many large HVDC transmissions projects all over the world are using MMC technology. Different power and voltage levels can be achieved by the MMC scalability, and they can be used with deferent variable semiconductor parameters. Also, multilevel waveform expandability to any number of voltages steps can be achieved in order to reduce harmonic distortion. Some multilevel inverter disadvantages in the previous chapter can be avoided by the MMC. The main idea and the operation principle of a MMC can be explained step by step, as will be seen, by assuming that two controllable DC voltage sources, to which the AC side is connected in between, are connected to the DC side of the converter as shown in Figure 10. Each DC source represents one arm of the converter, and both arms are called legs of the converter, which correspond to one phase. The criterion for controllable voltage sources is that their voltage sums have to match the constant DC bus. Since the voltage balance between two arms is required, that leads to the value of the voltage source in the lower arm decreasing at the same time that the value in the upper arm has to be decreased and vice versa. Because of balancing voltage between two arms, the connected load then ideally shares their currents equally.

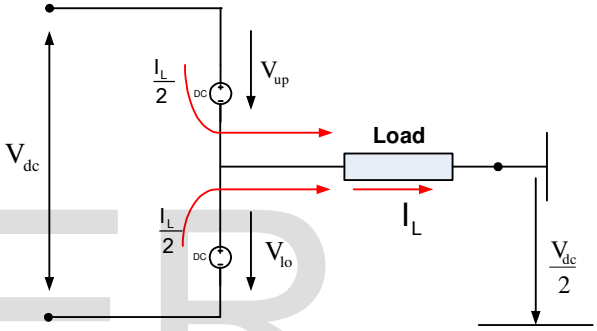

Fig. 10. MMC concept with two controllable voltage sources

Several identical constant voltage sources can be added in each arm, which can be inserted or bypassed depending on the status of switches in order to acquire a finite number of voltage levels. Since the use of a large number of DC sources is not recommended, capacitors in this case can be used instead. Each capacitor has two switches, one of which inserts the capacitor and the other bypasses the capacitor and is called the submodule. If the converter has a number of N submodules per arm, each of them will supply a voltage of Vdc/N, where Vdc is the DC bus. In that case and in order to have a constant voltage in the DC bus, N modules for one arm have to be connected and N modules for the other arm have to be bypassed. In this way, a total number of N+1 levels will be achieved. The capacitors cannot provide a constant voltage when they connected or bypassed the circuit. Also, a capacitor voltage varies according to the direction of the current when it is inserted in the arm. Therefore, a specific algorithm, which will be explained in detail in the next chapter, is used to charge and discharge submodules capacitors in order to avoid low charge or over charge for the capacitors. Because of the current transient due to unequal voltages between legs converters, an inductor is placed in each arm. The final single-phase MMC circuit is shown in Figure 11, and the respective three-phase in Figure 12.

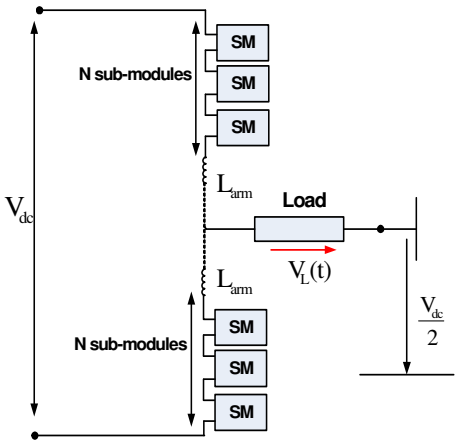

Fig. 11 Single-phase MMC circuit capacitors

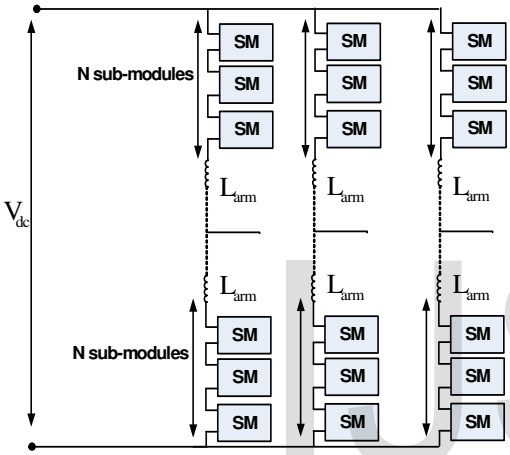

Fig. 12. Three-phase MMC circuit capacitors

The submodule is the main part of a Modular Multilevel Converter. Figure 13 shows the submodule half bridge scheme. As can be seen from Figure 13, the final configuration of each submodule, which contains a DC storage capacitor C; a half-bridge composed of two switching elements T1, which is inserted into the capacitor; and T2, which is bypassing the capacitor, with the freewheeling diodes D1 and D2.

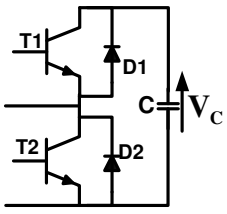

Fig. 13 MMC submodule

The number of the submodules connected in the series and on the converter size determines the capacitor's nominal voltage. The rating of the switching devices is determined by how much of the nominal voltage. Insulated-Gate Bipolar Transistors (IGBTs) are used for high-power applications. It is possible to operate the submodule in two different states when a special control can be applied to the switching elements, which are shown in Figure 14.

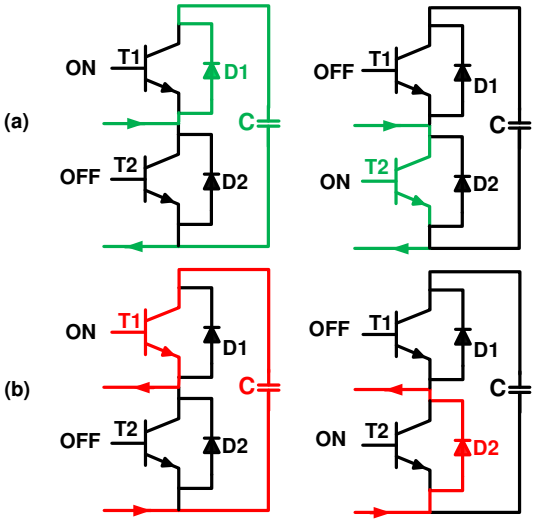

Fig. 14. (a) Positive and (b) Negative currents flow inside a MMC submodule

The green line indicates that the current flows from the DC side in the direction of the AC terminals. The red line indicates that the current flows in the opposite direction. If both the switches are OFF, the capacitor will be charged through the freewheeling diode D1, in the green flow. In the red flow, the capacitor will be bypassed when the current passes through the diode D2. The voltage of the capacitor is applied across the terminals of the submodule when T1 is turned on. In the green flow, the capacitor can be charged through D1; in the other case, the capacitor will be discharged through T1. The terminals of the submodule will be short-circuited when T2 is turned on and the current flows through T2 for a positive direction or flows through D2 for negative direction. The capacitor keeps its state of charge and its voltage remains unchanged when it has bypass status. Therefore, each of the submodules can be controlled separately by using these switching statuses. Table 3 summarizes the submodule action as described above.

TABLE3
SWITCHING STATES FOR EACH SUBMODULE

T1	T2	D1	D2	Current direction	Capacitor state	Output voltage
OFF	ON	OFF	OFF	$I_{arm}>0$	Uncharged (bypassed)	0
OFF	OFF	OFF	ON	$I_{arm}<0$	Uncharged (bypassed)	0
OFF	OFF	ON	OFF	$I_{arm}>0$	Charging	V_C
ON	OFF	OFF	OFF	$I_{arm}<0$	Discharging	V_C

Each leg represents one phase for MMC. Each leg consists of an upper arm and a lower arm. Each arm has a number of N submodules connected in series and the arm inductor Larm. To get a sinusoidal voltage at the AC terminals, the two arms of each leg can be controlled separately in order to obtain a balancing voltage across the AC terminal. That can be

achieved when the number of inserted submodules from one arm equals the number of bypassed submodules from the other arm. Capacitor voltage for each submodule, which is equal to the DC bus voltage divided by the number of submodules per arm, stresses the switching devices. Because of the difference between the three DC leg voltages in normal operation, the arm inductor is inserted in order to dampen the balancing currents between the three phases by using special control methods, which will be explained in next chapter. Also, it is used to decrease and limit the effects of the faults currents.

6 FTT Simulation Results for NPCMLI, CCMLI, CHMLI and MMC

The studies above were performed with 3-level, 5-level, 7-level, 9-level, 11-level, 13-level, 15-level, 17-level, 19-level, 21-level, 23-level and 25-level multilevel inverters for further comparison for NPCMLI, CCMLI, CHMLI and MMC. Table 4 shows line-to-neutral voltage and current THD. Figure 15 shows voltage THD for NPCMLI, Figure 16 shows voltage THD for CCMLI and Figure 17 shows voltage THD for CHMLI and Figure 18 shows voltage THD for MMC. It is obvious that MMC is the best to reduce THD as can be seen in Figure 19.

TABLE 4
ODD NUMBER FROM 3-LEVEL TO 25-LEVEL NPCMLI, CCMLI, CHMLI, AND MMC TOTAL HARMONICS DISTORTION

Type of Multi-level Inv. / Number of levels n	NPCMLI Voltage THD %	CCMLI Voltage THD %	CHMLI Voltage THD %	MMC Voltage THD %
3-level	52.34	52.24	52.13	43.69
5-level	27.01	26.95	26.18	22.72
7-level	18.3	18.25	18.18	15.5
9-level	13.75	13.72	13.59	11.78
11-level	11.12	11.09	10.87	9.57
13-level	9.38	9.36	9.22	8.16
15-level	8.01	8.02	7.58	7
17-level	6.76	6.88	6.40	6
19-level	6.39	6.56	7.18	5.77
21- level	5.72	6.10	5.22	5.31
23- level	4.96	5.42	5.16	4.7
25- level	4.71	5.11	4.92	4.57

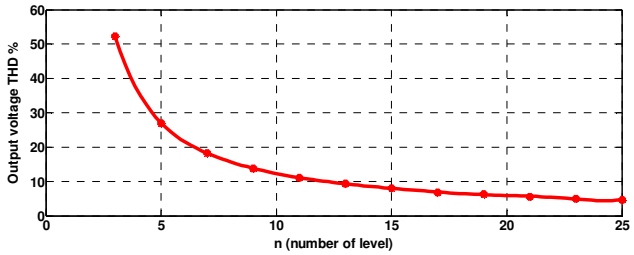

Fig. 15. Output voltage THD for NPCMLI

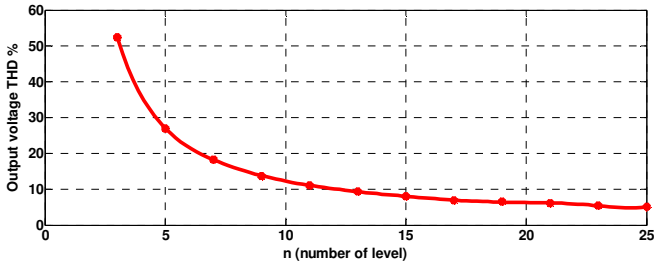

Fig. 16. Output voltage THD for CCMLI

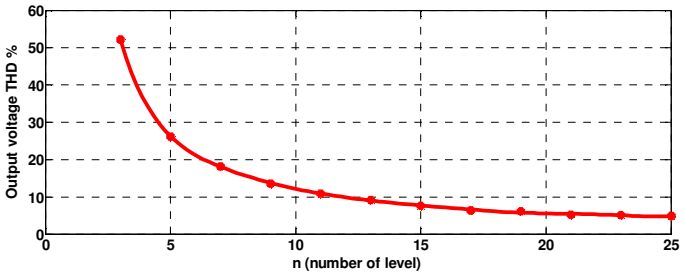

Fig. 17. Output voltage THD for CHMLI

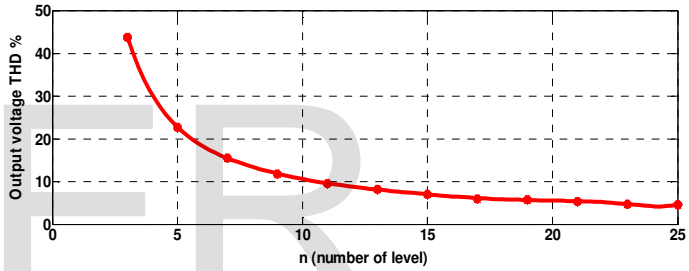

Fig. 18. Output voltage THD for MMC

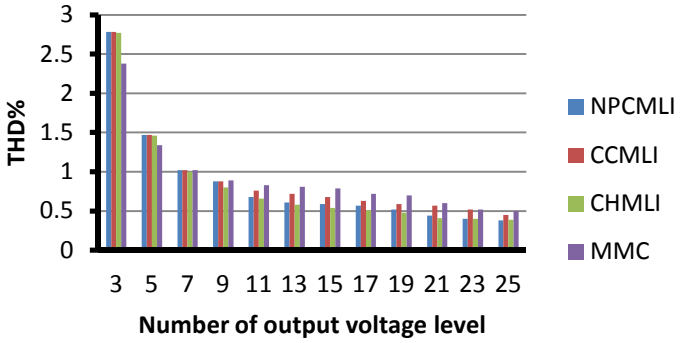

Fig. 19. Comprehensive comparison for THD for four types of MLI in this paper

7 Components Rating Comparison of Multilevel Inverters

Table 5 shows the numbers of required components per level. All the values in the table are for individual cases. Figure 20 shows the component requirements as stated in Table 5, not taking into account the rating comparison between the inverters. The main consideration for each inverter is its lowest voltage and current rating. For MMC, Modules in both arms are connected or bypassed to create an

AC output voltage. So, for a number of voltage levels m the inverter needs n-1 = N number of submodules per arm, so 2(n - 1) = 2N submodules per phase-leg. Compared to the somewhat similar CHMLI topology, the modules in this MMC topology can only put out two voltages from upper and lower arms. The MMC topology does not need shared DC-capacitors in a DC-bus, but it does, however, require a DC-bus for circulating currents. These currents, however, can also circulate through other phase-legs. The two inductors, one in each arm in a phase-leg, are there to take up the voltage difference when modules are switched in and out. Table 5 can be written to figure out the comparison between MMC and multilevel inverters in chapter one. Figure 20 shows the component requirements as stated in Table 5.

TABLE 5
COMPONENT REQUIREMENTS FOR THE TOPOLOGIES FOR A THREE-PHASE SETUP. THE VOLTAGE/CURRENT LEVEL IS REPRESENTED BY N

Topology	NPCMLI	CCMLI	CHMLI	MMC
DC bus cap./Isolated sources	$3\,(n-1)$	$3\,(n-1)$	$3\,\frac{(n-1)}{2}$	$6\,(n-1)$
Main diodes	$6\,(n-1)$	$6\,(n-1)$	$6\,(n-1)$	$12\,(n-1)$
Main switches	$6\,(n-1)$	$6\,(n-1)$	$6\,(n-1)$	$12\,(n-1)$
Clamping diodes	$3\,(n-1)(n-2)$	0	0	0
Clamping capacitor	0	$\frac{3\,(n-1)(n-2)}{2}$	0	0

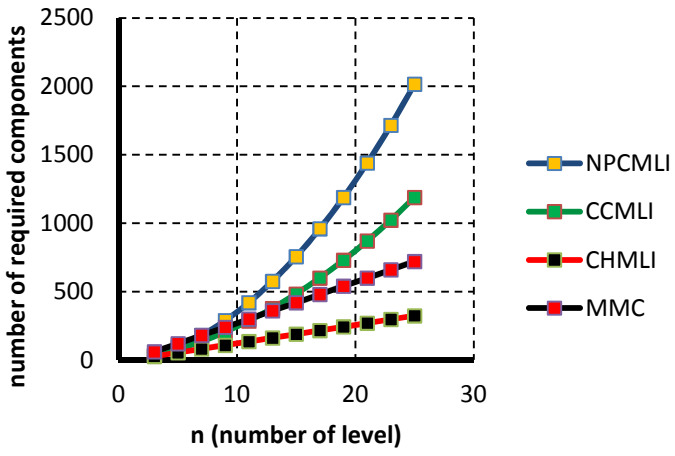

Fig. 20. Components needed for the topologies NPCMLI, CCMLI, CHMLI, and MMC

8 CONCLUSION

This paper has presented some topologies for multilevel inverters (MLI), all of which are known to have applications on the market. Every topology has been described in detail. The same sine wave pulse width modulation techniques that are used with the presented topologies have also been presented. Topology comparisons, such as numbers of components and their ratings, have been presented and show that multilevel inverters compete with inverters in the area of voltage ratings for their components (diodes, switches and such). Even though the number of components needed for multilevel inverters can be very high, as has been shown, they are used at a wide range of power ratings. The simulations in this chapter have presented results of the output waveforms for both voltage and current concerning both the voltage THD and current THD for the Multilevel Diode Clamped/Neutral Point Inverter (NPCMLI), Multilevel Capacitor Clamped/Flying Capacitor Inverter (CCMLI) and Cascade H-Bridge Multilevel Inverter (CHMLI) and Modular Multilevel Converter (MMC). It has also been shown that by increasing the output voltage level, THD can be reduced. Additionally, it has been shown that high voltage levels in the MLI are not needed for lower THD to be noticeable. Together with low switching frequencies, multilevel inverters can be used in applications for lower THD. To summarize the results of this chapter, it has been shown through simulations that multilevel inverters can be used to get lower THD for both output voltage and current. A higher number of components must be used, but these can be of a kind with lower voltage ratings, depending on the number of voltage levels used in the multilevel inverter. It seems that the main reason to use multilevel inverters is to reduce the THD so that fewer filters need to be used. Also this chapter explained the most important Advantages and Disadvantages of the Topologies for NPCMLI, CCMLI and CHMLI..

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